REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 1 through 19 are pending in this application. Claims 1 through 7 and claims 15 through 19 remain presented for examination. Claims 8 through 14 are withdrawn without prejudice to future prosecution. No new claims have been added.

SECTION 112 ISSUES

In the Office Action, claims 2 through 4 and claims 9 through 11 stand rejected under 35 U.S.C. §112, second paragraph. Applicants respectfully traverse.

Applicants respectfully point out that claims 9 through 11 are withdrawn from consideration as being drawn to a non-elected invention. Applicants presume the above rejection under 35 U.S.C. §112, second paragraph is instead intended to reject elected claim 16, which recites in pertinent part "gate area".

In an effort to more particularly and distinctly claim the present invention, applicants have amended claims 2 through 4 to now recite in pertinent part "gate region material". Claim 16 has been amended to now recite in pertinent part "gate region". Applicants believe that this terminology is now in agreement with the exemplary "gate region" disclosed in reference to Figure 1 (gate region 110) and in reference to Figure 5 (gate region 510). Applicants submit that the recitations of "gate region material" and "gate region" in claims 2, 3, 4, and 16 are not now indefinite when read in light of the specification and drawings.

Furthermore, applicants have amended the discussion on page 11 of the specification, in connection with Figure 7, to correct typographical errors, where "gate region 110" was erroneously labeled "gate area 110" and also where "gate region 510" was erroneously labeled "gate area 510". This correction brings this portion of the specification into agreement with the terminology "gate region 110" first used in connection with the discussion of Figure 1, and the terminology "gate region 510" first used in connection with the discussion of Figure 5. Applicants submit that no new matter has been introduced by this correction.

SECTION 103 ISSUES

In the Office Action, claims 1 through 7 and claims 15 through 19 stand rejected under 35 U.S.C. §103(a) as being anticipated by, among other references, *Stein, et al.*, U.S. patent number 4,055,837 (Hereinafter *Stein*). Applicants respectfully traverse.

Independent claim 1 recites in pertinent part "a *metal-oxide-semiconductor transistor* with a shifted flat band magnitude." Independent claim 15 recites in pertinent part "means for shifting a flat band magnitude in a *metal-oxide-semiconductor transistor*". (Applicants emphasis added.)

The Office Action stated that "*Stein* describes an apparatus (device) including a MOS transistor (fig. 1 31, col. 2 lines 7-8) with a shifted band flat band magnitude (col. 7 lines 32-35)". Applicants respectfully submit that *Stein* at Figure 1 actually discloses *two distinct*

structures, a metal-oxide-semiconductor (MOS) transistor, item reference 1, and a stand-alone metal-nitride-oxide-semiconductor (MNOS) capacitor, item reference 2. Specifically, *Stein* recites at column 2, lines 6 through 11:

> A single-transistor memory element, as best seen in FIG. 1, comprises a transistor 1 and a capacitor means 2 connected in series. The transistor 1 is a MOS field-effect transistor. The capacitor means 2 comprises a capacitor whose dielectric comprises rechargeable states, being a MNOS capacitor.

Any reference to a shifted flat band magnitude within *Stein* is in connection to *MNOS capacitor* 2, and never in connection with *MOS transistor* 1.

The Office Action reference to *Stein* column 7, lines 32 through 35, is clearly in regards to a capacitor, not a MOS transistor. Claim 20 of *Stein* recites in pertinent parts "for the operation of a single-transistor memory element ... comprising a write line, a transistor, and a capacitor ... such that where of an information '0' is stored in said capacitor a shifting of a flat-band voltage occurs ... ." This recitation indicates that it is *within the capacitor*, and not *within the transistor*, that any shifting of a flat-band voltage occurs.

Similarly claim 19 of *Stein* recites "such that flat-band voltage of said capacitor is shifted" (column 7, lines 8 and 9), and claim 22 of *Stein* recites "and in a case of the shifted flat-band voltage of the capacitor" (column 8, lines 23 and 24). Within the specification of Stein, applicants point out at column 2, line 68, through column 3,

line2, the following recitation: "[t]his means that the states ('traps') of the MNOS capacitor are recharged and that the flat-band voltage of the capacitor is shifted." Similarly *Stein* recites at column 3, lines 34 through 37, "a reloading of the states in the dielectric of the memory capacitor will be effected causing a prospective shift in the flat-band voltage." Thus *Stein* only discloses a "shift of a flat-band voltage" in relation to a *capacitor*, and never in relation to a *transistor*. However, claim 1 of the present application recites in pertinent part "a metal-oxide-semiconductor *transistor with a shifted flat band magnitude.*" (Applicants emphasis added.) *Stein* discloses no such metal-oxide-semiconductor *transistor with a shifted flat band magnitude*. Therefore, applicants submit that the invention of claim 1 is not anticipated by *Stein*.

For this reason, applicants submit that the invention of claim 1 is not anticipated by *Stein*, and should be allowed as distinguishable over the cited art of record.

Claims 2 through 7 depend from independent claim 1. Since independent claim 1 is believed allowable, applicants submit that claims 2 through 7 are also allowable.

As independent claim 15 was rejected "for reasons stated under claims 1-5 above", and since claim 1 is believed allowable, applicants submit that claim 15 is also allowable over the cited art of record. Since claims 16 through 19 depend from claim 15, and since claim 15 is believed allowable, applicants submit that claims 16 through 19 are also allowable.

SUMMARY

Applicants believe that all pending claims are allowable over the cited art of record. Applicants therefore respectfully request that all pending claims 1 through 7 and 15 through 19 be allowed.

If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to contact applicant's representative, Dennis A. Nicholls, at (408) 765-5789.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

Date: 5 March, 2002

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CHANGE TO SPECIFICATION

VERSION WITH MARKINGS TO SHOW CHANGES

The following is a copy of the two paragraphs beginning at page 10, line 21 and extending through page 11, line 15, marked up to show all the changes relative to the previous version of the two paragraphs:

In one embodiment of the present invention, the shifting of the location of the flat band by about 0.48 volts may be accomplished by the use of the PMOS transistor 500 of Figure 5. In order to move the flat band magnitude from about 1.5 volts to about 1.98 volts, a change of about 0.48 volts, one embodiment changes the threshold voltage Vt by changing the work function of the material comprising the gate region [area] 510. The p+ poly-silicon gate region [area] 110, which has a work function of approximately – 0.56 volts, is replaced by a p+ platinum-silicide gate region [area] 510, which has a work function of approximately – 1.04 volts.

In alternate embodiments, other gate materials such as tantalum nitrate (TaN), iridium (Ir), nickel (Ni), or arsenic (As) may be used to obtain different flat band voltages, depending upon the magnitude of the voltage to be decoupled. These materials may be used by themselves or as dopants in silicon, poly-silicon, or other materials. In further embodiments, the flat band magnitude may be changed by changing the dopant levels of substrate 502 and channel area 508. Finally, in alternate embodiments when Vcc differs from 0.4 volts, a

corresponding shift in flat band magnitude may be obtained by replacing the gate region [area] 510 material or by changing the dopant levels in the substrate 502 and channel area 508.

CLAIMS

VERSION WITH MARKINGS TO SHOW CHANGES

2. The apparatus of claim 1, wherein said metal-oxide-semiconductor includes a gate region [area] material with a work function less than – 0.56 volts.

3. The apparatus of claim 2, wherein said gate region [area] material is platinum silicate.

4. The apparatus of claim 2, wherein said gate region [area] material is selected from the group consisting of tantalum nitrate, iridium, nickel, and arsenic.

16. The apparatus of claim 15, wherein said means for shifting includes a gate region [area] with a material whose work function is less than – 0.56 volts.